IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A data transfer control circuit for carrying out data transfer by using a plurality of bus masters, comprising:

a data bus connected to a peripheral apparatus, said data bus having a plurality of unit data buses, each of which transfers data concurrently;

a plurality of bus masters configured to send a request signal requesting a use of each of said unit data buses and to use said unit data buses requested when a request by means of said request signal is granted; and

[[a]] one bus controller configured to split-control said unit data buses for said plurality of bus masters by giving a grant signal which grants the use of each of said unit data buses in accordance with said request signal, wherein

the request signal has ~~a data field~~ an operand comprising a plurality of bits, each of said plurality of bits corresponding to a respective one of said unit data buses, and said bus controller grants the use of each of said unit data buses specified by the bits of said request signal.

Claim 2 (Previously Presented): The data transfer control circuit according to claim 1, wherein:

said bus controller sends the grant signal to said bus masters based on a bus release requesting signal requesting release of said unit data buses.

Claim 3 (Previously Presented): The data transfer control circuit according to claim 1, wherein:

said bus controller includes a monitor circuit for monitoring availability of said unit data buses.

Claim 4 (Previously Presented): The data transfer control circuit according to claim 3, wherein:

said bus controller judges whether said unit data buses of said data bus are available based on a monitoring result of said monitor circuit, and when said unit data buses are available, said bus controller provides the grant signal of the use of said unit data buses to said bus master.

Claim 5 (Previously Presented): The data transfer control circuit according to claim 3, wherein:

said bus controller sends a state signal indicating the availability of said unit data buses to each of said bus masters based on a monitoring result of said monitor circuit.

Claim 6 (Original): The data transfer control circuit according to claim 1, wherein:

said request signal includes information specifying each unit data bus in said data bus.

Claim 7 (Original): The data transfer control circuit according to claim 1, wherein:

said request signal includes information specifying the number of the unit data buses in said data bus.

Claim 8 (Currently Amended): An information processing system for carrying out data transfer by using a plurality of bus masters, comprising:

a peripheral apparatus;

a data bus connected to a peripheral apparatus, said data bus having a plurality of unit data buses, each of which transfers data concurrently;

a plurality of bus masters configured to send a request signal requesting a use of each of said unit data buses and to use said unit data buses requested when a request by means of said request signal is granted; and

[[a]] one bus controller configured to split-control said unit data buses for said plurality of bus masters by giving a grant signal which grants the use of each of said unit data buses in accordance with said request signal, wherein

the request signal has ~~a data field~~ an operand comprising a plurality of bits, each of which said plurality of bits corresponding to respective one of said unit data buses, and said bus controller grants the use of each of said unit data buses specified by the bits of said request signal.

Claim 9 (Previously Presented): The information processing system according to claim 8, wherein:

said bus controller sends the grant signal to said bus masters based on a bus release requesting signal requesting a release of said unit data buses.

Claim 10 (Previously Presented): The information processing system according to claim 8, wherein:

said bus controller includes a monitor circuit for monitoring availability of said unit data buses.

Claim 11 (Previously Presented): The information processing system according to claim 10, wherein:

said bus controller judges whether said unit data buses of said data bus are available based on a monitoring result of said monitor circuit, and when said unit data buses are available, said bus controller gives the grant signal of the use of said unit data buses to said bus master.

Claim 12 (Previously Presented): The information processing system according to claim 10, wherein:

said bus controller sends a state signal indicating the availability of said unit data buses to each of said bus masters based on a monitoring result of said monitor circuit.

Claim 13 (Original): The information processing system according to claim 8, wherein:

said request signal includes information specifying each unit data bus in said data bus.

Claim 14 (Original): The information processing system according to claim 8, wherein:

said request signal includes information specifying the number of the unit data buses in said data bus.

Claim 15 (Currently Amended): A method of carrying out data transfer through a data bus having a plurality of unit data buses by using a plurality of bus masters, comprising:

generating a request signal requesting a use of each of unit data buses in each of a

plurality of bus masters and sending said each request signal to a bus controller, said data bus being connected to a peripheral apparatus and each of said unit data buses transfers data concurrently;

sending, in response to said request signal, a grant signal granting the use of each of said unit data buses in accordance with said request signal; and

occupying said unit data buses granted by said grant signal, and carrying out data transfer by using the unit data buses thus occupied, wherein

the request signal has ~~a data field~~ an operand comprising a plurality of bits, each of said plurality of bits corresponding to a respective one of said unit data buses, and said bus controller grants the use of each of said unit data buses specified by the bits of said request signal.

Claim 16 (Previously Presented): The method according to claim 15, wherein:

sending of said grant signal includes sending said grant signal based on a bus release requesting signal requesting a release of said unit data buses.

Claim 17 (Previously Presented): The method according to claim 15, further comprising:

monitoring availability of said unit data buses.

Claim 18 (Previously Presented): The method according to claim 17, wherein:

sending of said grant signal includes sending the grant signal based on the availability of said unit data buses.

Claim 19 (Previously Presented): The method according to claim 17, further comprising:

sending a state signal indicating the availability of said unit data buses to each of said bus masters.

Claim 20 (Previously Presented): The method according to claim 15, wherein:

generating of said request signal includes generating said request signal including information specifying each unit data bus in said data bus or information specifying the number of the unit data buses in said data bus.

Claim 21 (Currently Amended): A data transfer control circuit for carrying out data transfer by using a plurality of bus masters, comprising:

a data bus connected to a peripheral apparatus, said data bus having a plurality of unit data buses, each of which transfers data concurrently;

a plurality of bus masters configured to send a request signal requesting a use of each of said unit data buses and to use said unit data buses requested in response to a bus master select signal which indicates the current bus master to which said grant signal is given; and

[[a]] one bus controller configured to split-control said unit data buses for said plurality of bus masters by giving a grant signal which grants the use of each of said unit data bus in accordance with said request signal, and sending said bus master select signal to each of said bus masters, wherein

the request signal has ~~a data field~~ an operand comprising a plurality of bits, each of said plurality of bits corresponding to a respective one of said unit data buses, and said bus controller grants the use of each of said unit buses specified by the bits of said request signal.

Claim 22 (Currently Amended): An information processing system for carrying out data transfer by using a plurality of bus masters, comprising:

a peripheral apparatus;

a data bus connected to a peripheral apparatus, said data bus having a plurality of unit data buses, each of which transfers data concurrently;

a plurality of bus masters configured to send a request signal requesting a use of each of said unit data buses and to use said unit data buses requested in response to a bus master select signal which indicates the current bus master to which said grant signal is given; and

[[a]] one bus controller configured to split-control said unit data buses for said plurality of bus masters by giving a grant signal which grants the use of each of said unit data buses in accordance with said request signal, and sending said bus master select signal to each of said bus masters, wherein

the request signal has ~~a data field~~ an operand comprising a plurality of bits, each of said plurality of bits corresponding to a respective one of said unit data buses, and said bus controller grants the use of each of said unit buses specified by the bits of said request signal.

Claim 23. (Currently Amended): A method of carrying out data transfer through a data bus having a plurality of unit data buses by using a plurality of bus masters, comprising:

generating a request signal requesting a use of each of unit data buses in each of a plurality of bus masters and sending, in response to a bus master select signal which indicates the current bus master to which said grant signal is given, said each request signal to a bus controller, said data bus being connected to a peripheral apparatus and each of said unit data buses transferring data concurrently;

sending, in response to said request signal, a grant signal granting the use of each of said unit data buses in accordance with said request signal, and sending said bus master select signal to each of said bus masters; and

occupying said unit data buses granted by said grant signal, and carrying out data transfer by using the unit data buses thus occupied, wherein

the request signal has ~~a data field~~ an operand comprising a plurality of bits, each of said plurality of bits corresponding to a respective one of said unit data buses, and said bus controller grants the use of each of said unit buses specified by the bits of said request signal.

Claims 24 – 26 (Cancelled)

Claim 27 (New): The data transfer control circuit according to claim 1, wherein said bus controller send a bus master selection signal to all of said bus masters along with said grant signal, said selection signal indicating a bus master by which said grant signal is to be received.

Claim 28 (New): The information processing system according to claim 8, wherein said bus controller send a bus master selection signal to all of said bus masters along with said grant signal, said selection signal indicating a bus master by which said grant signal is to be received.